# What is your Dream Job?

Come chat with our friendly ambassadors today!

MEDIATEK

Scan the code for available openings!

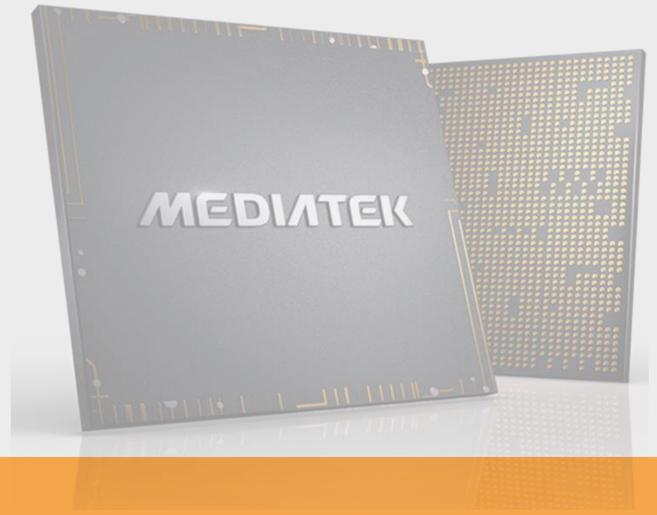
# Design Verification Engineer

**What you will do**

- As deep sub-micron process requires longer research cycle and higher manufacture cost, DV(design verification) has become an inevitable part of design group in Mediatek chip development flow. It included: integrated simulation/verification env development, big data analysis and efficiency improvement, bus fabric / EMI (External memory interface ) / Low power functions verification plan and implementation Need to build up verification plan/bench and continuously improve methodology, and you will understand both detail scenario and global view of cell phone/ASIC operating schemes Need to leverage the latest EDA tool and concept to accomplish the verification plan.

**Are you the right talent?**

- Bachelor’s degree in Electrical Engineering, Computer Engineering or related
- Dedication to continuous self-developing and learning new technologies
- Good knowledge of chip design flow and EDA tools
- Strong coding skills in C/C++, Perl, Python, and Unix/Linux shell



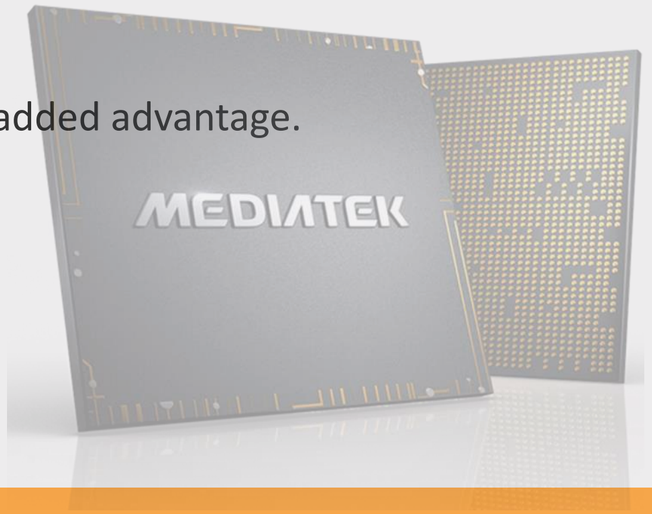
# Analog / RF Design Engineer

**What you will do**

- Design of RF/Analog/Mixed-signal IC circuit blocks / IPs based on specifications (performance, area, power consumption).
- Realize IC layout with floor planning and performance considerations (with layout engineers).
- Testing & Debugging of IC prototypes (with system verification engineers).
- Support of IC to mass production ready.
- Continual support / debug of field related issues or customer IC rejects.
- IC design and performance documentation.

**Are you the right talent?**

- Bachelor's Degree / Master’s Degree in EEE (major in IC Design).
- Knowledge of RF/analog designs through final year project and internship are an added advantage.
- Training will be provided.



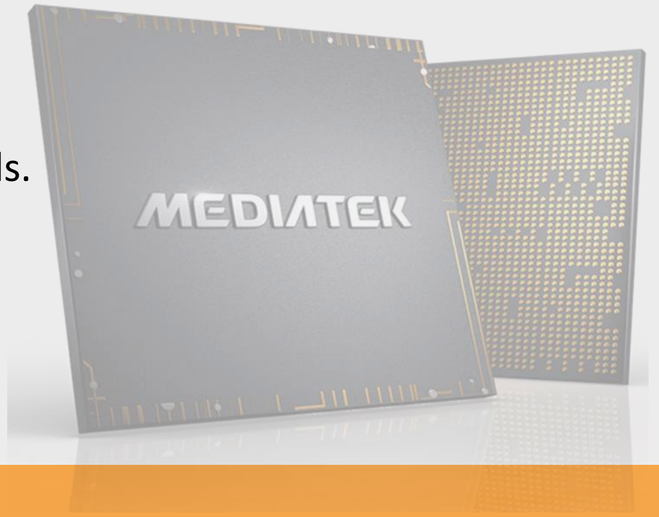
# SOC Digital Design Engineer

**What you will do**

- Develops the logic design, RTL coding, and simulation for an SoC design and integrates logic of IP blocks and subsystems into a full chip SoC or discrete component design.
- Participates in the definition of architecture and microarchitecture features of the block being designed.
- Performs quality checks in various logic design aspects ranging from RTL to timing/power convergence.
- Applies various strategies, tools, and methods to write RTL and optimize logic to qualify the design to meet power, performance, area, and timing goals as well as design integrity for physical implementation.
- Reviews the verification plan and implementation to ensure design features are verified correctly and resolves and implements corrective measures for failing RTL tests to ensure correctness of features.
- Follows secure development practices to address the security threat model and security objects within the design.
- Works with IP providers to integrate and validate IPs at the SoC level. Drives quality assurance compliance for smooth IP to SoC handoff.

**Are you the right talent?**

- The ideal candidate will have the desire and ability to learn logic and validation skills.
- Bachelor’s degree in Electrical Engineering, Computer Engineering or related



# Physical Verification Sign-off Engineer

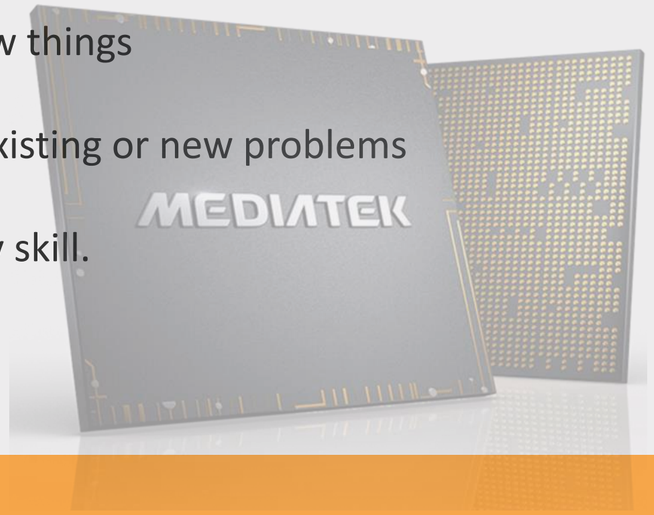
**What you will do**

When you join us, you'll work alongside with experienced engineers who'll mentor and guide you.
You will be involved in:

- Execute design rule checks on real chip design
- Debug real issues related to design rule checks happening at full chip integration
- Do basic reporting on physical verification issues
- Basic project management/project risk assessment reporting
- Basic scripting automation

**Are you the right talent?**

- Pursuing a degree in Electrical/Electronics/Computer Science Engineering
- Must be an independent worker and  have a strong drive to learn and pick up new things
- Able to communicate well and handle cross team collaboration
- Be willing to explore unfamiliar territory and try to seek innovative solutions to existing or new problems
- Able to demonstrate critical thinking when faced with difficult situations
- Having IC layout experience and scripting knowledge is a plus but not a necessary skill.



# Software Engineer (Physical Verification)

**What you will do**

- Involve in various stages of the software development lifecycle, including requirements gathering, design and implementation, and deployment.
- Develop, improve and maintain CAD flow & methodology for ensuring correct electrical and logical functionality and manufacturability.
- Work closely with team members and develop solutions using Open-Source Software technology.
- Directly involved in our physical verification methodology efforts, collaborating right alongside our internal multi-functional teams to ensure that our products achieve best-in-class PPA (Power, Performance & Area) and time-to-market.

**Are you the right talent?**

- You are pursuing a degree in Computer, Software or Engineering related studies
- You have knowledge in one of the programming languages and are willing to increase skills in this area (Python, Perl, Tcl or JavaScript)
- You have a passion in coding and eager to learn
- You enjoy collaborating with others to find innovative solutions
- You think logically, willing to self-learn and research, and take a creative approach to problem solving
- You have basic IC design knowledge (this is a plus but not mandatory)

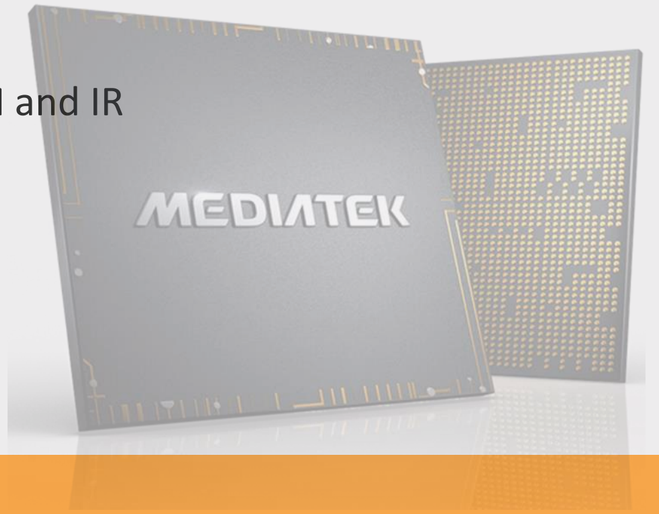
# Full Custom Layout Engineer

**What you will do**

- Implement top quality layout which meet the specifications set forth by designers and layout leads while meeting the project objectives and fast paced milestones
- Diligently perform all physical & reliability verifications (DRC/LVS/ERC/etc.) on the layout designs and ensure the database is fully compliant with all requirements of tape-out flow
- Work closely and communicate effectively with multi-functional teams and multi-site to constantly optimize layout for better power, performance, area and schedule
- Responsible for in-house IP/library developments

**Are you the right talent?**

- Bachelor’s degree in Electrical/Electronic Engineering
- Has transistor level knowledge for circuits and device layout structure
- Understands analog layout fundamentals, such as floorplan, device matching, EM and IR
- Have a good grasp of DRM of advanced node CMOS technologies
- Team player and effective in cross-team communication and time management
- Proficiency in script programming (e.g. Tcl, Perl or C-shell) is a plus



# IC Physical Design Engineer

**What you will do**

- IC physical design of 12nm/6nm/4nm and below world leading advanced process chip, from RTL to GDS.
- Block owner, take block of 2~3 Million instances, working on Synthesis/APR(auto place and route)/Signoff
- Block coordinator role for more than 5~10 blocks, solving the critical issue and give the solution to block owners.
- TOP role for the complicated hierarchical chip (more than 20 Million instances plus 500+ macros), doing floorplan and partition, responsible for full chip tape out

**Are you the right talent?**

- Basic knowledge of electronic design or IC design, internship experience in related area is preferred.
- Basic knowledge of UNIX/LINUX env and capable of at least one of the following programming language: C/C++, Python, TCL, Perl
- Good communication and teamwork spirit, eager to learn new technologies and willing to take challenges

# Memory Design Automation Engineer

**What you will do**

- Own cutting edge technology node's SRAM compiler design and deliver best quality of design kit
- Seamlessly collaborate with SRAM design team to achieve highest quality of design kit delivery
- Responsible for data analysis and platform development of memory usage big data
- Responsible for physical verification (DRC/ERC/LVS/ANT) on SRAM compiler
- Responsible for spice simulation on timing, power and noise on SRAM compiler
- Responsible for QA check and development on SRAM compiler

**Are you the right talent?**

- Bachelor/Master Degree in Electrical and Electronic Engineering/Computer Engineering/Computer Science
- Multi-task capability and strong self-driven characteristics to meet challenging schedules
- Proficient with Perl, Shell, Python, C/C++ languages, knowledge with machine learning algorithm and infrastructure is an added advantage
- Strong interpersonal skills to work with team members with multi-cultural environment
- Knowledge of high performance, low power SRAM/ROM and VLSI design is an added advantage
- Fresh graduates are welcome

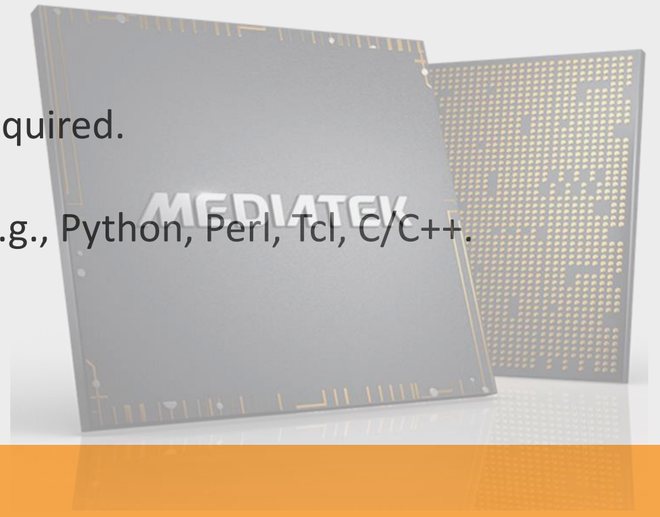
# Standard Cell Library Characterization Engineer

**What you will do**

- Responsible for Standard Cell Library Characterization for leading edge process node (7nm/5nm/4nm/3nm), as the pioneer to setup design platform for MediaTek projects.
- Perform timing/power/constraint/noise modeling for >15K logic circuit for one process node.
- Perform LVF modeling, statistical variation simulation and analysis
- Co-work with designer and tool vendors to tackle modelling difficulties, and solve the accuracy and runtime issues, especially for customized circuit cannot be handled by commercial tools.
- Responsible for flow development, new kits enablement and evaluation, e.g., EM characterization, Aging characterization.
- Data trend analysis in machine learning for circuit performance and power assessment.
- Involve in sub-threshold voltage circuit characterization and verify functionality with expected PPA

**Are you the right talent?**

- Engineering/Computer Engineering/Computer Science, no prior experience is required.
- Basic knowledge of IC design and circuit design.
- Basic knowledge of UNIX/LINUX environment and any programming language, e.g., Python, Perl, Tcl, C/C++.
- Familiar with foundation IP (Std-cell, Memory, I/O) design and/or CAD is a plus.
- Knowledge of data analysis, machine learning is a plus.



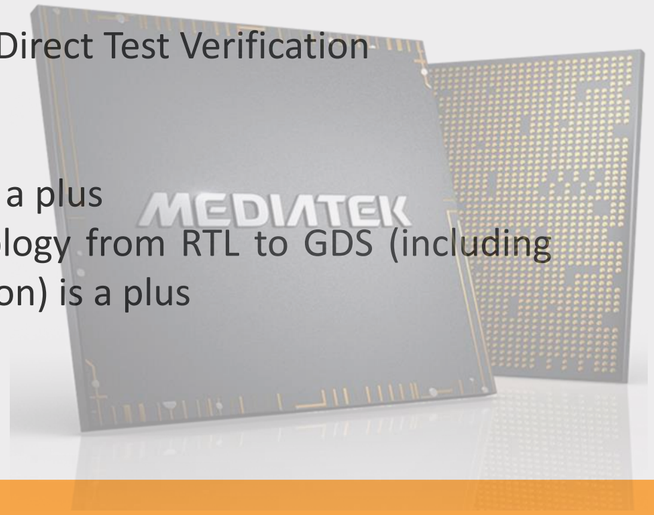
# Timing Signoff Engineer

**What you will do**

- Work on timing sign off, convergence, automations and methodology development.
- Timing analysis, validation and debug across multiple PVT conditions using PT/Tempus.
- Run Primetime and/or Tempus for STA flow optimization and Spice to STA correlation.
- Evaluate multiple timing methodologies/tools on different designs and technology nodes.
- Experience in design automation using TCL/Perl/Python
- Familiar with process technology enablement: Spice simulation Hspice/FineSim, Monte Carlo. Silicon to spice model correlation.
- Strong expertise in STA timing analysis basics, AOCV/POCV/LVF concepts, CTS, defining and managing timing constraints, Latch transparency handling, 0-cycle, multi-cycle path handling

**Are you the right talent?**

- Bachelor's/Master's Degree in Electrical/Computer Engineering
- Knowledge in ARM/IMG/Tensilica Processor Familiarity, Silicon Debug and/or Functional/Direct Test Verification
- Familiar with assertion-based verification (SVA) & System Verilog language
- Knowledge in Processor verification, FPGA verification and/or Formal verification
- Familiar with Synopsys ICC (preferred) or Cadence or Magma tools from netlists to GDS is a plus
- Knowledge in graphics processor implementation/power reduction flows and methodology from RTL to GDS (including synthesis, floor-planning, placement, CTS, routing, timing optimization, physical verification) is a plus
- Knowledge of high-speed/low power IP and custom circuit design is a plus
- Familiar with power noise and reliability tools such as Redhawk and Voltus
- Good communication and scripting skills



# GPU/APU Physical Implementation Engineer

**What you will do**

- Responsible for physical design and development activities of MediaTek's Ghz ARM/Imagination-based graphics processors, AI processors and neural network DSP
- Involve in activities encompass physical design and analysis of complex and timing-critical graphics processor AI processors and neural network DSP
- Technical disciplines include synthesis, floor-planning, place and route, RC extraction, timing and power optimization
- Implementation flow development
- Work closely with MediaTek's colleagues in Taiwan and Singapore in implementation methodology co-development and flow deployment

**Are you the right talent?**

- Bachelor's/Master's Degree in Electrical/Computer Engineering
- Knowledge in ARM/IMG/Tensilica Processor Familiarity, Silicon Debug and/or Functional/Direct Test Verification
- Familiar with assertion-based verification (SVA) & System Verilog language
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